

2019 Field Programmable Gate Array Design

LAB Schedule

Week	Lab	Topic
9/16	Lab0	An introduction to Verilog How to run simulation on Vivado
9/23	Lab1	Sequential Circuit Design On FPGA and Hardware Debug
9/30	Lab2	Block Design and IP
10/7	Lab3	SoC Design with Zynq Processor
10/21	Lab4	Custom AXI IP Package
11/4	Lab5	Block RAM
11/18	Lab6	Python on Zynq
12/2	Lab7	Design with DSP IP
1. Tool : Xilinx Vivado 2. FPGA Development Board : PYNQ-Z2 3. LAB Github : https://github.com/ncku-vlsilab/2019_FPGA_Design		